



REMARKS

The specification has been amended to correct minor typographical errors. No new matter has been entered. Pursuant to 37 CFR 1.121, a marked copy of the amended specification paragraphs showing the changes made therein accompanies this Amendment.

Turning to the rejection of claim 37 under 35 USC § 112 for being indefinite, the Examiner's rejection is in error. Claim 37 clearly states that the trenches are formed using a first photoresist pattern. Since the first photoresist pattern layer is also recited in claim 37, it is clear where the trenches are formed. Thus, Applicant respectfully submits that the Examiner's § 112 rejection is in error.

Turning to the rejection of claims 37 and 39-41 under 35 USC § 103(a) as being obvious over Applicant's admitted prior art (APA) in view of the newly cited Patent to Gilbert et al. (U.S. Patent No. 5,885,856), as the Examiner is no doubt aware, in order for a proper § 103 rejection to be formed, there must exist in the art some motivation to combine the references. In rejecting the claims as obvious from the APA in view of Gilbert et al., the Examiner acknowledges that the APA does not teach forming a first photoresist pattern layer, a first photomask and forming a trench in the semiconductor substrate by an etching process using the first photoresist pattern layer. However, the Examiner takes the position that this missing teaching is provided by Gilbert et al. While Gilbert et al. may form isolation trenches to provide electrical isolation between various components of the integrated circuit (col. 2, lines 42-46), Gilbert et al. does not teach forming these trenches to correspond to the active area patterns in the dummy area patterns as required by independent claim 37 of the instant invention. In fact, Gilbert et al. teaches against the claimed invention in warning that the

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dummy structures must not intersect or come into contact with well boundaries (col. 3, lines 10-19), and proposes a method for determining which regions are active regions and which regions are dummy regions (col. 4, lines 19-51). Nowhere does Gilbert et al. teach or suggest using a first masking layer defining the active regions and dummy regions to form trenches, and using a second masking layer corresponding to the first masking layer to form active gates and dummy gates as required by Applicant's claims. Thus, Gilbert et al. cannot be combined with the Applicant's APA to render obvious claim 37 or claims 39-41 which depend thereon.

Turning to the rejection of claim 38 as obvious from the APA in view of Gilbert et al. and further in view of the newly cited Patent to Shimomura et al. (U.S. Patent No. 6,140,687), claim 38 is dependent on claim 37. The deficiencies of the combination of the APA and Gilbert et al. vis-à-vis claim 37 are discussed above. It is not seen that Shimomura et al. supplies the missing teachings to the APA/Gilbert et al. combination to achieve or render obvious claim 37, or claim 38 which depends thereon. Shimomura et al. has been cited specifically to teach that it is conventional to form circular shaped gates. Even assuming *arguendo* the Examiner's characterization of Shimomura et al., the more basic and essential teachings missing from the APA/Gilbert et al. combination, as discussed above, are not supplied by Shimomura et al. Thus, no combination of the APA, Gilbert et al. and Shimomura et al. could achieve or render obvious claims 37 or 38 which depends thereon.

Having dealt with all the objections raised by the Examiner, it is believed that the Application now is in order for allowance. Early and favorable action are respectfully requested.

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Amendment D

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,

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MARKED AMENDED SPECIFICATION PARAGRAPH:

Paragraph beginning at page 5, line 23:

Finally, referring to Fig. 3C, the photoresist layer 203 is removed. Thus, the gate conductive layer [102] 202 has gate patterns [G1] P1 and [G2] P2 corresponding to the gate patterns GP1 and GP2, respectively, and also, has dummy gates DG corresponding to the dummy gate patterns DP.

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